Altera Arria 10 SoC Development Platform
Product Brief (HTK-A10-SOC-MOD)

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PRODUCT DEVELOPMENT SERVICES

Features

- Altera Arria 10 SoC standalone platform
- Networking centric design
- FMC mezzanine slot for application flexibility
- Compact 8.5” x 6.75” module
- 1U enclosure available
- Complete FPGA support package available
- Full suite of Ethernet IP cores available

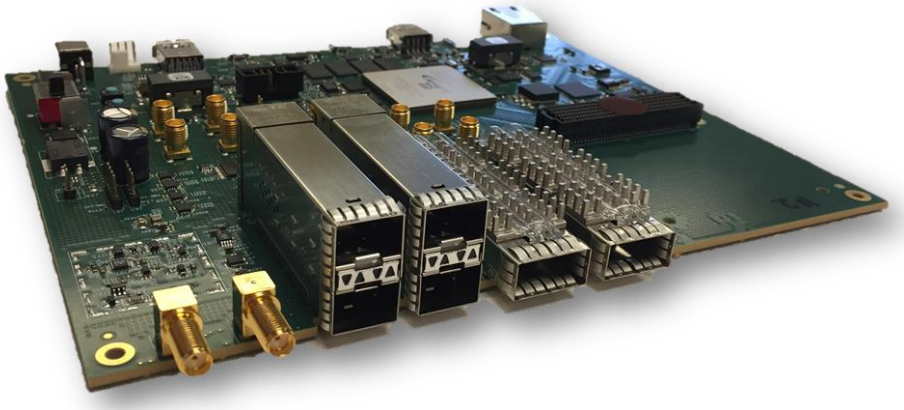
Applications

- Rapid prototyping
- Low to mid volume production
- OEM and white label branding available

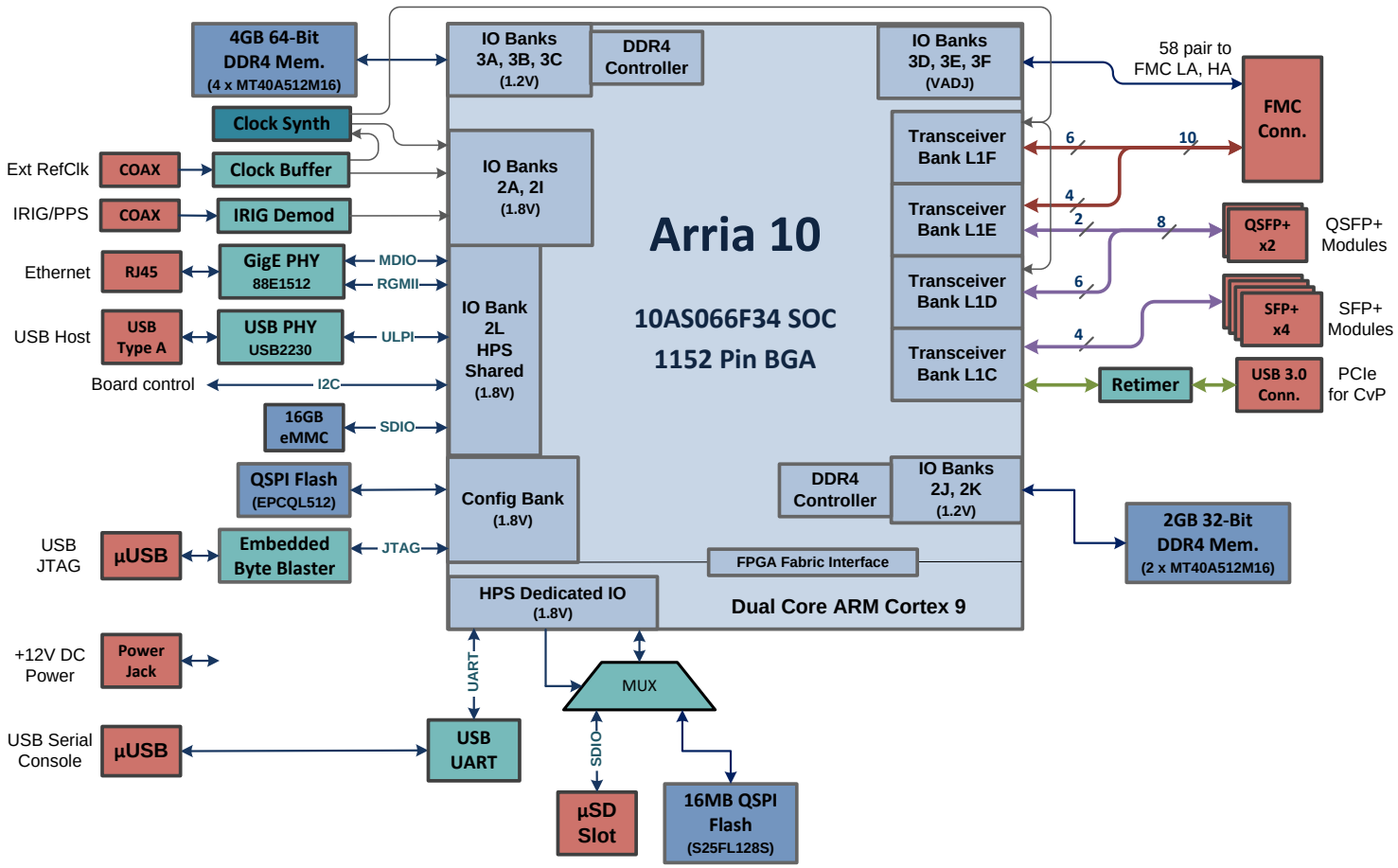
Target Markets

- Wireline / Wireless / RF Communications
- Signal Processing / Imaging Processing
- 1G / 10G / 40G Wire-Speed Encryption / Decryption
- High Performance Computing
- High-speed trading and Financial

HIGHLY INTEGRATED, LOW-COST, FEATURE RICH, NETWORKING CENTRIC DEVELOPMENT PLATFORM



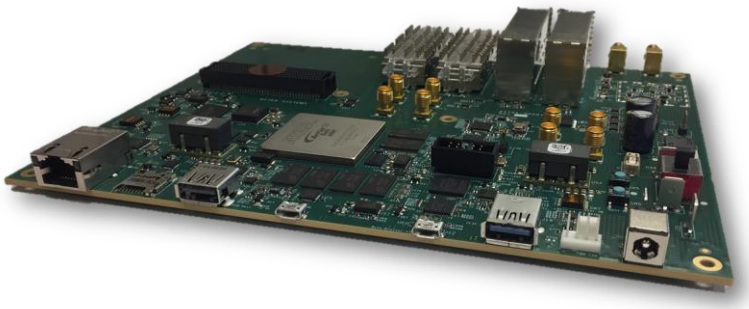
The Altera Arria SoC (10AS066-2E) based development platform is a network centric design with a single FMC mezzanine slot for application flexibility. All network and user interfaces are located on one edge and control / power on the opposite edge allowing for quick custom enclosure solutions. An integrated USB Byteblaster II is included for easy lab debugging.



HTK-A10-SOC-MOD

Front Panel Interfaces:

- Dual QSPF+ ports for 40G interfaces
- Quad SFP+ ports for 10G/1G interfaces
- FMC interface with partial HPC support; All LA, HA and 10 Serdes lanes routed to FPGA
- Max VADJ of 1.8V on LA, HA signals; DIP switch selectable for 1.2V, 1.5V and 1.8V
- 5 – 200MHz external reference clock input
- 1PPS or IRIG-A/B/G input



Rear Panel Control and Debug Interfaces:

- GiGE interface to the Arria SoC HPS
- Type A USB 2.0 Host port to the Arria SoC HPS
- Micro-USB port for serial console access to the HPS processor
- Micro-USB port for integrated ByteBlaster II access to the FPGA / SoC JTAG port
- 1x PCIe Gen2 slave (CvP capable) interface via USB3.0 interface connector

Power Tree:

- Single 12V power connecter
- Adheres to Altera's recommended Arria10 power-up and power-down sequencing

HPS Configuration and Memory Interfaces:

- HPS side 2Gbyte 32-bit DDR4 DRAM bank
- On-board 1Gbit QSPI Flash memory
- On-board socket for uSD memory card
- On-board 16Gbyte eMMC storage device
- DIP switch selectable booting from on-board QSPI, uSD card, or FPGA fabric including CvP

FPGA Configuration and Memory Interfaces:

- FPGA side 4Gbyte 64-bit DDR4 DRAM bank
- 512Mbit QSPI Flash device
- On-board PCIe connection to allow CvP configuration of the FPGA fabric over PCIe

Clock and Synchronization functions:

- Flexible clocking to allow operation of interfaces at multiple rates
- Front panel input for 5MHz-200MHz external reference clock
- Front panel IRIG A/B/G (AM and DLCS) or 1PPS interface

On-board Development and Debug Support:

- On-board reset pushbutton and configuration DIP switches
- Multiple on-board diagnostic and status LED's
- On-board I2C monitor access to main power regulators
- On-board I2C access to clock synthesizer and programmable oscillators
- Module and SoC on-die temperature monitoring

Customization options available. Contact us for details.

Links

http://www.mantaro.com/products/development-boards/arria-10-soc-module.htm
http://www.mantaro.com/products/fpga-ip-cores.htm

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Product Ordering Codes

Dev Platform: HTK-A10-SOC-MOD-0662E

1U Enclosure: HTK-A10-SOC-ENCL

FPGA Support Package: HTK-A10-SOC-FSP